



700MHz-2700MHz, 50W, 28V RF Power LDMOS FETs

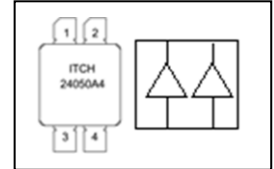
Description

The ITCH24050A4 is a 50-watt , internally matched LDMOS FET, designed for cellular base station and ISM applications with frequencies from 700MHz to 2700 MHz.

Its 4-lead configuration enables the flexibility to design the power amplifier in form of single ended, push pull, 90 degree hybrid, for either class AB/C or Doherty applications.

It is also featured by the application to share the same general purpose PCB layout for any narrow band application within 0.7-2.7GHz only with modification of bill of materials to fit specific narrow band use.

ITCH24050A4



- Typical Performance of 920-960MHz (On Innegration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 320$ mA , Pulse Width =10us, Duty Cycle =12%.

Freq(MHz)	P1(dBm)	P1(W)	Gain@P1(dB)	P3(dBm)	P3(W)	Eff(%)@P3
920	49.47	88.5	19.7	49.97	99.3	64.36
940	49.09	81	19.6	49.80	95.5	65.62
960	48.52	67.9	19.3	49.52	89.5	64.26

- Typical Performance of 2400-2500MHz (On Innegration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 300$ mA , Pulse Width =10us, Duty Cycle =12%.

Freq(MHz)	P1(dBm)	P1(W)	Gain@P1(dB)	P3(dBm)	P3(W)	Eff(%)@P3
2400	48.75	75	15.4	49.53	89.7	53.65
2450	48.15	65.3	15.7	49.05	80.3	54.52
2500	47.66	58.3	15.6	48.61	72.6	53.28

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.9	°C/W



$T_C=85^{\circ}\text{C}$, $T_J=200^{\circ}\text{C}$, DC test			
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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (per Section)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$; $I_{DS}=1\text{mA}$	V_{DSS}	65			V
Zero Gate Voltage Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}			1	μA
Gate--Source Leakage Current	$V_{GS} = 9\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}			1	μA
Gate Threshold Voltage	$V_{DS} = 28\text{V}$, $I_D = 300\ \mu\text{A}$	$V_{GS(th)}$		1.75		V
Gate Quiescent Voltage	$V_{DS} = 28\text{ V}$, $I_{DS} = 300\ \text{mA}$, Measured in Functional Test	$V_{GS(O)}$		2.7		V

Pulse CW Signal performance of per Section (In Innogrator Test Fixture, 50 ohm system): $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 400\ \text{mA}$, $f = 920\text{-}960\ \text{MHz}$, Pulse CW, Pulse Width=12 us, Duty cycle=10% .

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_p		20		dB
Drain Efficiency@P1dB	η_D		60		%
1dB Compression Point	P_{-1dB}		60		W
Input Return Loss	IRL		-7		dB

Load Mismatch of per Section (On Innogrator Test Fixture, 50 ohm system): $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 300\ \text{mA}$, $f = 960\ \text{MHz}$

VSWR 10:1 at 50W Pulsed CW Output Power	No Device Degradation
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Table 5. Single Section Load-Pull Performance:

$V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 100\ \text{mA}$, Pulsed CW, Pulse Width=200 us, Duty cycle=20% .

ITCH24050A4 2400MHz	Freq (MHz)	VDD (V)	Idq (mA)	Zsource (ohms)	Zload (ohms)	Pout (dBm)	Gain (dB)	Eff (%)
MXP	2400	28	100	10.9-j*23.1	3.2-j*4.5	47.13	13.89	64.15
MXE	2400	28	100	10.9-j*23.1	2.0-j*3.0	45.70	15.67	70.53
Trade Off	2400	28	100	10.9-j*23.1	2.7-j*3.9	46.93	14.54	66.19
ITCH24050A4 2450MHz	Freq (MHz)	VDD (V)	Idq (mA)	Zsource (ohms)	Zload (ohms)	Pout (dBm)	Gain (dB)	Eff (%)
MXP	2450	28	100	13.6-j*25.0	2.9-j*4.8	47.09	14.04	64.35
MXE	2450	28	100	13.6-j*25.0	1.8-j*3.4	45.60	15.88	70.32
Trade Off	2450	28	100	13.6-j*25.0	2.5-j*4.3	46.89	14.59	66.10
ITCH24050A4 2500MHz	Freq (MHz)	VDD (V)	Idq (mA)	Zsource (ohms)	Zload (ohms)	Pout (dBm)	Gain (dB)	Eff (%)
MXP	2500	28	100	18.1-j*28.1	3.0-j*4.9	47.05	14.12	65.28
MXE	2500	28	100	18.1-j*28.1	1.8-j*3.7	45.52	15.96	70.25
Trade Off	2500	28	100	18.1-j*28.1	2.5-j*4.5	46.85	14.74	67.01



Figure 1: Gain and Efficiency as function of output power

Test signal: pulse width: 100us, duty cycle: 10%, Vds=28V, Idq=300mA

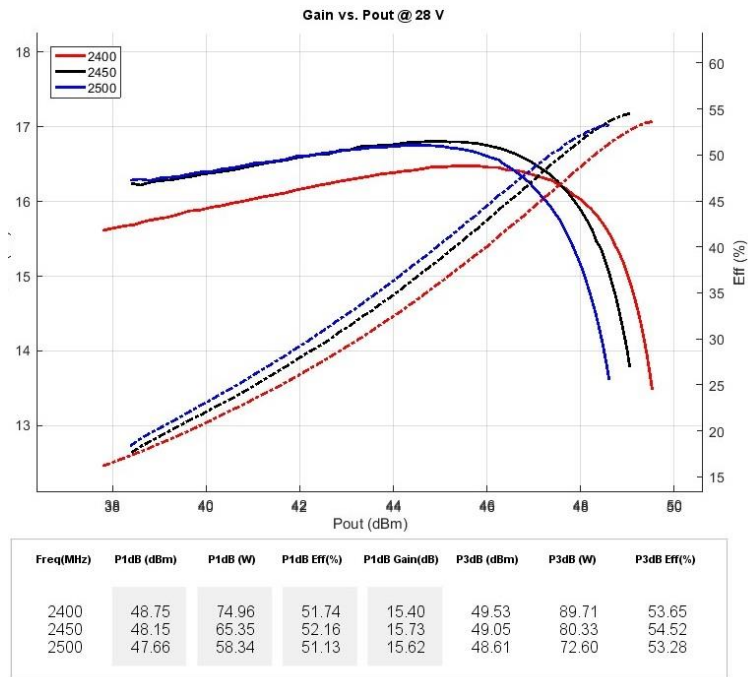


Figure 2: WCDMA performance at 2.4-2.5GHz

Test signal: 1 Carrier WCDMA (PAR=10.5dB @ 0.01% probability), Vds=28V, Idq=300mA

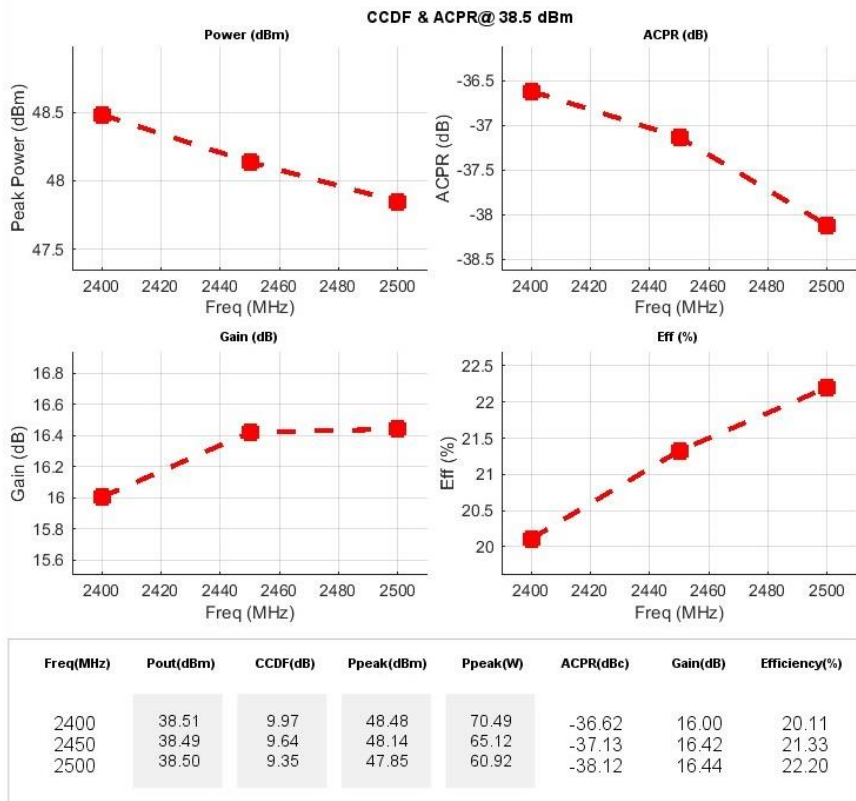


Figure 3: Photo of fixture and bill of materials for 2.4-2.5GHz

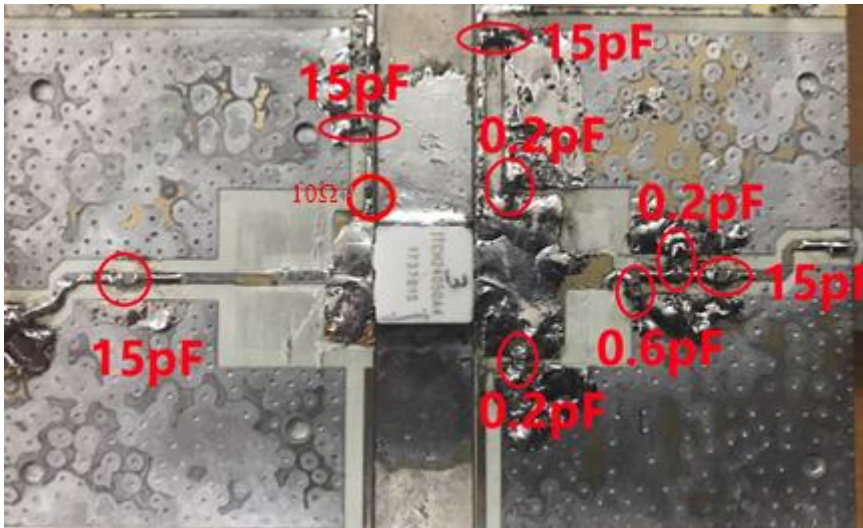
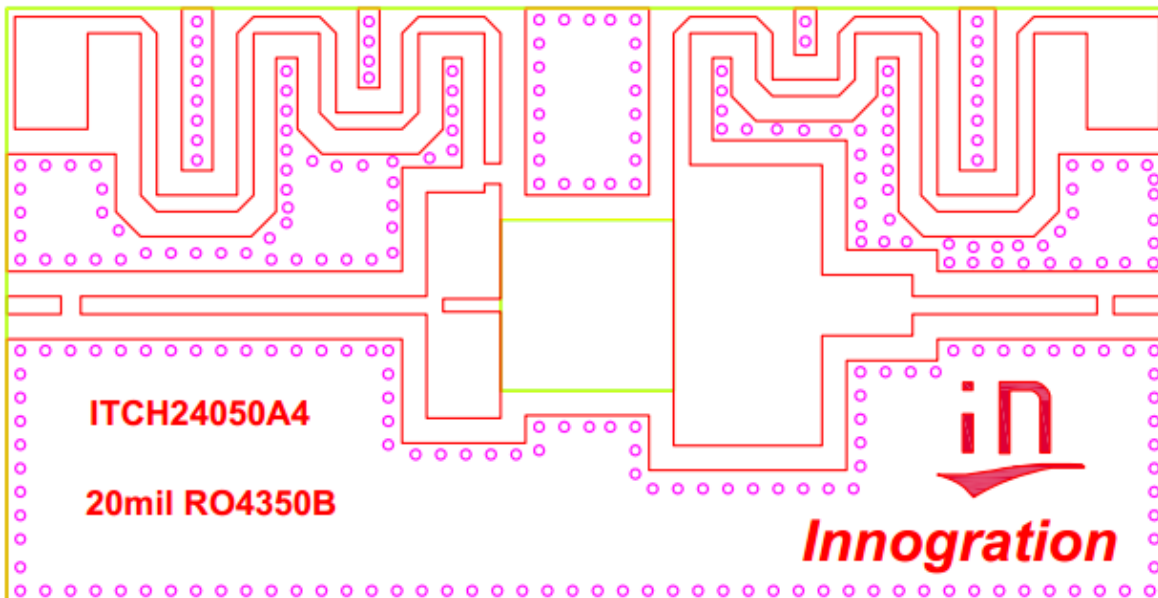


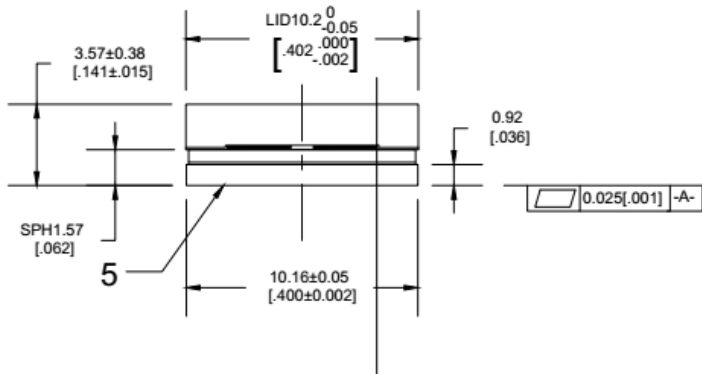
Figure 4: layout of the general purpose PCB (applicable to any narrow band within 0.7-2.7GHz)



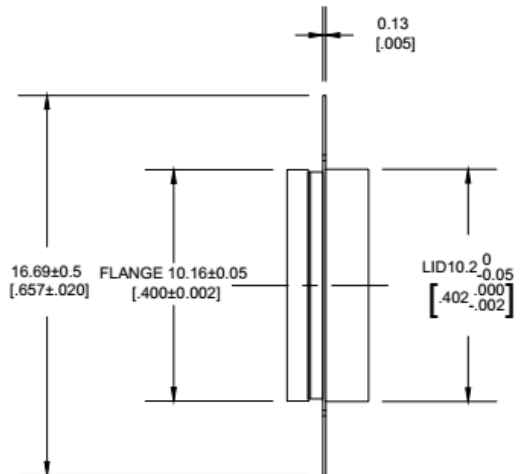
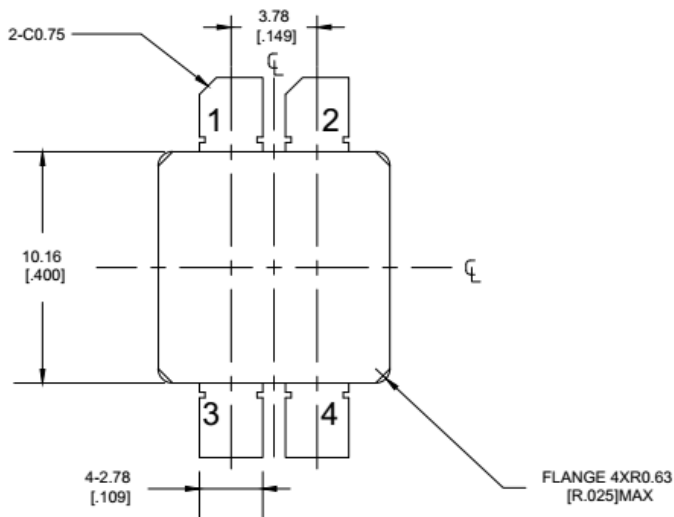


Package Outline

Earless Flanged ceramic package; 2 leads



Pin Connection				
Drain		Gate		Source
1	2	3	4	5



Unit: MM [Inches]

Unless specified tolerances: ±0.125MM



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2017/8/31	Rev 1.0	Preliminary Datasheet
2017/9/21	Rev 2.0	Add test data of 900MHz, 2400MHz

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